Deed of Donation with Order no. 3/2025

concluded in accordance with the provisions of Section 2055 et seq. of Act No. 89/2012 Coll., the Civil Code, as amended.

1. Parties

CyberSecurity Hub, z.s. ("**CSHub**"), a registered institute existing under the laws of Czech Republic, having its registered office at Šumavská 416/15, 602 00 Brno, Czech Republic, company ID: 09705163
Delegated: Roman Čermák, M.Sc., MBA, Director
hereinafter referred to as the "**Donor**"

and

Masaryk University ("MU"), a public university existing under the laws of Czech Republic, having its registered office at Žerotínovo nám. 617/9/7, 601 77 Brno, Czech Republic, ID: 00216224
hereinafter referred to as the "**Donee**", enter into this deed of donation with the order (hereinafter also referred to as "**Deed**")

2. DECLARATION OF THE PARTIES

1.1 CSHub as the Donor declares he signed the *Agreement between NARLabs and CSHub* on May 17, 2024 to implement Advanced Chip Design Research Center (hereinafter also referred to as **ACDRC**) in the Czech Republic. Annex 1 to the Agreement between NARLabs and CSHub defines the **Working Plan** of ACDRC.

1.2 CSHub further declares he signed *Deed of Donation with Order* (hereinafter also referred to as **Primary Deed**) between Taipei Economic and Cultural Office, Prague (TECO) and CSHub on June 5, 2024, and therefore he shall receive a donation for the implementation of the ACDRC project.

1.3 The Donor and Donee (hereinafter also referred to as **Parties**) declare they signed the *Consortium Agreement on Implementation of Advanced Chip Design Research Center Between Cybersecurity Hub, Brno University of Technology, Czech Technical University, and Masaryk University* on December 12, 2024 including all of its Appendices (hereinafter also referred to as **Consortium Agreement**). The purpose of the Consortium Agreement is to establish an academic consortium (referred to herein as Consortium) on the Czech side to implement ACDRC.

1.4 According to Consortium Agreement, paragraph 2.5, a part of the funding received by CSHub on the Czech side shall be further distributed to consortium parties to finance the collaboration in the Consortium leading to implementation of the ACDRC.

1.5 This Deed is a partial implementation of the Consortium Agreement which also defines the terms and condition of this Deed.

3. SUBJECT OF THE DEED

3.1 With this Deed, the Donor will donate a financial amount of **CZK 4 852 350** (hereinafter referred to as the "**Donation**") to the Donee with an order for the partial implementation of the ACDRC project. The Donee accepts the Donation under this Deed on the terms and conditions set out in this the Primary Deed and this Deed. In case of discrepancy between Primary Deed and this Deed, the terms and conditions stated In the Primary Deed apply first.

3.2 The partial implementation is done in form of **Subprojects** under Work Package 3 as defined by the ACDRC Working Plan, a list of activities of the Donee and their incurred costs are described in Annex 1 to this Deed. These activities tasks from the ACDRC WP3 contribute to the overall goals of ACDRC.

3.3 The Donation defined in paragraph 2.1 of this Article shall be transferred to the Donee's bank account no.: **85636621/0100 (VS: 25332025)** in Komerční banka, a.s., after the conclusion of this Deed as one-time payment. The payment will be transferred without delays after this Deed comes into force and no later than 30 days after the signing of this Deed.

3.4 The Donor and the Donee agree that the conversion rate from USD to CZK is 22.559, based on the CNB conversion rate of June 7, 2024, when the donor received a donation from TECO.

4. TERMS AND CONDITIONS

A. General Terms

The Donee fulfills specific tasks from the ACDRC Working Plan and contributes to the overall goals of ACDRC. General Terms are defined in the Consortium Agreement unless specified otherwise in this Deed. General rules specifying the purpose of the Deed, but also non-eligible costs are defined in the Primary Deed (attached as Appendix 3 to the Consortium Agreement), under 4. Determination of the Order.

B. Coordinators:

The Parties will each designate a coordinator whose responsibility will be to develop formal agreements related to specific activities that may result from this Deed. Each Party designates the following people to facilitate and administer the fulfillment of this Deed:

a. Donor: xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

b. Donee: xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

C. Amendment:

This Deed and appendices may be amended as agreed upon by both Parties. Any amendments or modifications to this Deed shall be accepted by both Parties in writing, using an Amendment Document. Matters not included in the Deed, but directly related to it, may be addressed by an Amendment Document, and executed by both Parties. Any such agreement shall be appended to this Deed. This Deed is executed in electronic form with electronic signatures of both parties.

5. Register of contracts

By signing this Deed, both Parties confirm that they are aware that for the Donee, the Deed is subject to the obligation to publish it pursuant to Act. No. 340/2015 Coll., on the register of contracts, as amended. The Donor publishes this Deed.

IN WITNESS WHEREOF, both Parties have caused this Deed to be executed by their duly authorized representative.

Donor: CyberSecurity Hub, z.ú.	Donee: Masaryk University
09.06.2025	04.06.2025
(signed electronically) Roman Čermák, M.Sc., MBA Director	(signed electronically) prof. MUDr. Martin Bareš, Ph.D. rector

Annex 1: Description of the ACDRC Activities of the Donee according to 2.2

A. **Activities according to 2.2**

Title of the Subproject: Preparation of new training courses on validation and verification of silicon chips

Czech Consortium Partner (Donee): Masaryk Univerzity, Faculty of Informatics

Taiwanese Partners: ---

Project start date: 05/2025, **end date:** 12/27

Principal Investigator: xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Abstract (up to 200 words):
To foster innovation and respond to emerging industry needs, the project will develop and implement two cutting-edge training courses within the Computer Systems, Communication, and Security study program, under the Hardware Systems specialization at the Faculty of Informatics, Masaryk University. These courses are designed to equip students with advanced skills in chip design and related technologies, significantly enhancing their competitiveness and adaptability in the evolving job market.
As part of the project, course materials will be developed for the new courses taught: Validation of Silicon Chip Designs and Verification of Silicon Chip Designs. Both courses are being developed in close cooperation with the industrial partner Renesas and will be offered once per academic year.
The instruction will include practical exercises and workshops. To support effective teaching, it will be necessary to acquire suitable hardware and software, including FPGA development kits and software licenses for chip design and simulation environments.

Detailed description (up to 2000 words):
The core content of the courses has been consulted with our industrial partner Renesas. Their experts will assist in the course preparation to ensure it better meets the needs of the industry. Renesas, operating in the Czech Republic, designs and tests silicon chips and has many years of experience and expertise in this field.

<u>Proposed course content outline</u>:
1/ Verification of Silicon Chip Designs
- Design requirements -> VITEMs (Verification Plan)
- UVM based testbench showing examples of project testbench structure/tests
- Regression
- Coverage

2/ Validation of Silicon Chip Designs
- Test reuse from Verification
    - Verification Plan -> Validation Plan
- Building validation environment
    - Based on Validation plan
    - Collect all necessary laboratory instruments – manage calibration/rental

- Define requirements on DUT PCB
- FPGA design
    - IO interconnect generator (from high-level spreadsheet description)
    - Functional block examples
- Python environment setup
- Test examples (software-layered approach)
- Regression runs and results

As a part of the courses, students will learn more about the design of silicon chips and the process of their fabrication. They will be introduced to the basic methods of validation and verification for digital design. A prerequisite for enrolling in these courses will be the completion of two existing Hardware Description Language (Verilog) courses currently taught at the Faculty of Informatics.
For the purpose of practical exercises and testing, it will be necessary to purchase hardware. This will primarily include the acquisition of development kits with modern FPGA SoC systems and accessories such as external peripherals for testing designs, e.g., communication interfaces (SPI, I2C, etc.). For demonstrations and more demanding simulations, we will also acquire FPGA development boards with PCIe interface and suitable computers. To support development and demonstrations during instruction, we also plan to purchase digital analyzers and oscilloscopes.
The project will result in the creation of new teaching materials, including lectures and demonstration exercises. The courses will feature guest lectures by external industry partners and student excursions directly to companies. The main contributors to the course development will be Zdeněk Matěj and Jan Král. Additional support from Ph.D. students will be required for course preparation and subsequent teaching of practical exercises.

Planned staffing costs:
The involvement of the entire team is essential for the successful implementation of the project, and all members will be engaged throughout its duration. The cost calculation is based on the actual salaries of an associate professor and an assistant professor, as well as the average salaries of Ph.D. students at the Faculty of Informatics. It also includes all mandatory employer contributions, such as social and health insurance and contributions to the social fund.
- xxxxxxxxxxxxxx – 0.1 FTE (associate prof.)
- xxxxxxxxxxxxxx – 0.1 FTE (assistant prof.)
- Ph.D. student – 0.2 FTE
- Ph.D. student – 0.2 FTE
- Administration/project support/Ph.D. student – 0.1 FTE Total: 0.7 FTE – CZK **2 112 880**

Other planned costs necessary for the project implementation including explanation:
- **Student scholarship** for work beyond the scope of the project (especially necessary during the preparation phase) – **CZK 50 000**
- **Equipment** – **CZK 1 060 000** includes:
    - **Hardware**
        - Zynq UltraScale+ SoC kits (10 pcs – CZK 401 000 incl. VAT)
        - FPGA boards for PCs (CZK 281 000 incl. VAT)
        - educational kits and accessories, and computing equipment (CZK 118 000 incl. VAT)
    - **Software** – acquisition cost for Cadence, Synopsys (260 000 CZK incl. VAT)
- **Services (Licenses for software tools)** – CZK **659 000** (Cadence, Synopsys incl. VAT)
    - Within this category, we plan to purchase approximately 5x annual licenses of Cadence software and 3 annual licenses of Synopsys software for the entire duration of the project. The price was determined based on market research, and the exact number of licenses will be adjusted according to the specific requirements of the

courses planned. However, both software tools are essential for teaching in these courses.

- **Overhead** – 25% of direct costs

Milestones and deliverables:

Milestones:

- 02/26 – finalization of course preparation and exercises for Validation of Silicon Chip Designs
- 09/26 – finalization of course preparation and exercises for Verification of Silicon Chip Designs

Deliverables:

- 07/26 – study materials of Validation of Silicon Chip Designs
- 01/27 - study materials of Verification of Silicon Chip Designs
- Interim and final reports submitted annually according to the funder requirement

Detailed budget table

Personnel cost	2 112 880 CZK
Scholarship	50 000 CZK
Services (annual licenses - Cadence, Synopsys, etc.)	659 000 CZK
Equipment (Zynq UltraScale+ SoC kits; FPGA boards for PCs; educational kits and accessories, and computing equipment; SW tool Cadence, Synopsis -> acquisition costs)	1 060 000 CZK
Overheads (25%)	970 470 CZK
Total	**4 852 350 CZK**